REMARKS/ARGUMENTS

Original claims 1-13 remain in the application.

Claims 1-13 have been rejected.

New claims 14-18 have been added in this paper.

The Examiner has objected to claim 8 for "insufficient antecedent basis" for the term "said channel number pair". Applicants have amended claim 8 to overcome the Examiner's objection.

Claims 1-3 have been rejected under 35 U.S.C. 102 (b), as being anticipated by Riley. (US 5,907,539). To anticipate, "the reference must teach every aspect of the claimed invention either explicitly or impliedly. Any feature not directly taught must be inherently present." (M.P.E.P. 706.02) "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. V. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987) (M.P.E.P. 2131). "The identical invention must be shown in as complete detail as contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989) (M.P.E.P. 2131) "The elements must be arranged as required by the claim, but this is not an *ipsissimis verbis* test, i.e., identity of terminology is not required." In re Bond, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990) (M.P.E.P. 2131). With respect to independent claim 1, the Examiner has suggested that Riley teaches an apparatus for transferring multiplexed multiple multi-bit messages across a bit level network, including a "network interface configured to transmit and receive a message at a preselected one of a plurality of time-division multiplex addresses (see Fig. 21, Frame Identifiers/addresses in plurality of frames/messages) on each channel of a preselected channel set (see Fig. 21, pluralities of

serial multiplex time division slots (i.e. channels) forms into a frame (i.e. pre-selected channel set)". Applicants contend that Riley teaches a network interface for multiplexing a multi-bit message across a bit level network to a preselected one of a plurality of time-division multiplexed addresses at a rate of one message bit per consecutive data frame until the complete multi-bit message has been transmitted. Riley's Figure 21 is a timing diagram showing the relationship between the master clock signal 85 on clock line 44 (Fig. 1) and a data signal 87 on data line 46 (Fig. 1) at time slot 36, during three consecutive frames 62, 62', 62". It does not, as the Examiner has suggested, illustrate "preselected channel sets" as defined in the present invention. Further, the Examiner's comments suggest a misunderstanding of the elements claimed in the present invention with respect to the elements taught by Riley. The Examiner suggests that Riley's Frame Identifiers are addresses of the present invention, time division slots are the channels of the present invention, which is not absolutely true in either case. Riley uses the term "channel" (channel A or channel B) only as an input or output of a data link module 32. However, Riley indicates that each "channel" is associated with an address (Col. 7, lines 66-67), which is actually equivalent to one time slot on the clock bus (Col. 6, lines 8-9). The Examiner also suggests that Riley's time division slots form frames, which are the "preselected channel sets" of the present invention. A number of time division slots do form frames in both Riley and the present invention. However, Riley's frames are not equivalent to, nor do they function in the same manner as the "preselected channel sets" of the present invention. Each of the 256 bits of Riley's frame represent one address, while each channel of a channel set of the present invention is made up of some number of bits (16 or 32 bits in the representative embodiment) assigned to one address. The Examiner further suggest that Riley discloses "a memory in communication with said processor (see FIG. 16, Serial to Parallel Shift Register 496 stores the data, and it couples to Integrated circuit 80)". Applicants agree that Riley's shift register is in communication with the processor, however, it receives a multi-bit message at a rate of one bit per frame until the shift register is full, it does not receive a complete multi-bit message on a preselected channel set. For the reasons stated herein, Riley does not meet the

requirements set forth in the M.P.E.P. for an anticipation rejection of claim 1 under 35 U.S.C. 102, as suggested by the Examiner.

With respect to claim 2, applicants agree that Riley does teach a network interface having a clock signal and a data signal. However, since claim 2 is dependent from claim 1, it will be allowable if claim 1 is allowed according to the decision in *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988), "If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious."

With respect to claim 3, the data signal of Riley is multiplexed at one bit per frame to each address in a frame that is receiving data. It is not sent in a data stream of consecutive data bits as in the present invention. Therefore, Riley does not meet the conditions required for an anticipation rejection under 35 U.S.C. 102, as set forth in M.P.E.P. 706.02 and M.P.E.P. 2131.

Claims 4-13 have been rejected under 35 U.S.C. 103 (a), as being unpatentable over Riley (US 5,907,539) in view of Sakagami (US 5,329,525). According to M.P.E.P. 706.2(j) three basic criteria must be met for a *prima facie* obviousness rejection of claims under 35 U.S.C. §103(a). First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on the applicants disclosure. The 35 U.S.C. 103 (a) rejection of claims 4-13 relies on the 35 U.S.C. 102 (b) rejection of claim 1 based on Riley, which has been traversed above. The teaching of Sakagami relies on bit stream transmission of data, which is not taught, suggested or supported by bit level multiplexing of Riley. Further, the Examiner has suggested that the elements HD, ADS, SLP and AP of Sakagami constitute a "command segment" of the multi-bit message as required in the

present invention. In column 6, lines 26-30, Sakagami defines these as: HD a header signal indicating the start of data, ADS as address information, SLP as a sleep bit and AP as a parity bit. Applicants do not believe that theses elements, as defined by Sakagami, teach or suggest the "command segment" as claimed in the present invention. None of the elements of Sakagami teach or suggest what is to be done with the data provided in the "operand segment" of the multi-bit message. Therefore, there is no teaching or suggestion in the cited prior art for the Examiner's suggested combination.

In reply to the Office Action dated February 10, 2004, the objections and rejections set forth by the Examiner have been carefully considered. Applicants have made amended the drawings and the specification to correct unintentional errors with respect to reference numerals and consistency of terms. Amendments have also been made to the claims to overcome the Examiner's objections, to correct inadvertent errors and to more precisely define the invention. Applicants have also presented arguments herein to overcome the Examiner's rejections and believe that all pending claims are in condition for allowance. Applicants therefore respectfully request a favorable reconsideration and allowance of this Application.

Respectfully submitted,

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